NBS-DIO48

NuBus Digital I/O Interface

Hardware Reference Manual

Board Assembly 5010.010A

This page intentionally left blank

fishcamp engineering
4860 Ontario way
Santa Maria, CA 93455

TEL: (805) 345-2324
FAX: (805) 345-2325

Printed in U.S.A. January 1998

Limited Warranty

The NBS-DIO48 interface hardware is warranted to be free from defects in materials and workmanship for a period of 90 days from date of shipment from fishcamp engineering. Defects caused by misuse, abuse, or shipment are not covered.

Defective equipment that is subject to this limited warranty will be repaired or replaced at the option of fishcamp engineering if we are notified during the warranty period. The customer must obtain a Return Material Authorization (RMA) number before returning any equipment. Shipping costs from fishcamp engineering will be paid by fishcamp engineering. Equipment should be packaged in the original shipping container if possible, and the RMA number must be clearly marked on the outside of the package.

The information provided in this manual is believed to be correct, however fishcamp engineering assumes no responsibility for errors contained within. The software programs are provided "as is" without warranty of any kind, either expressed or implied.

No other warranty is expressed or implied. Fishcamp engineering shall not be liable or responsible for any kind of damages, including direct, indirect, special, incidental, or consequential damages, arising or resulting from its products, the use of its products, or the modification to its products. The warranty set forth above is exclusive and in lieu of all others, oral or written, express or implied.

The information covered in this manual is subject to change without notice.

Further Reading

For further information regarding the 82C55A Programmable Peripheral Interface chip used on the NBS-DIO48 card refer to:

Microsystem Components Handbook

Published by:

Intel

Intel Literature Sales
P.O. Box 58130
Santa Clara, CA 95052-8130

Order Number - 230843

Trademarks

This page intentionally left blank

Table of Contents

This page intentionally left blank

Section 1
Introduction

The fishcamp engineering model NBS-DIO48 interface board was designed to allow the interface of the Apple Macintosh II personal computer family to the many varied devices available today which have a parallel digital interface. The board plugs into any of the NuBus slots in the Macintosh computer. The NBS-DIO48 card has a high density 62-pin 'D' interface connector which protrudes out the back of the computer when the interface is installed. A total of 48 interface signals are available on the card and a variety of handshaking options are supported. Fused +5v power is available on the interface connector for use with external signal conditioning circuitry.

The NBS-DIO48 board was designed around the Intel 82C55A controller chip. An Apple Macintosh operating system compatible driver resides in PROM on the board allowing the user to program his/her application in conformance with the Mac's defined architecture. Routines allowing direct access to the internal registers of the 82C55A controller chips are included in the driver. All operating modes of the interface card are software configurable.

The rest of this manual describes the installation and operation of the NBS-DIO48 card along with presenting some technical information relating to the design of the card. This manual is a companion document to the NBS-DIO48 Software Reference Manual which should be consulted for information relating to the use of the software driver in the board's PROM.

Section 2
Installation

Installation of the NBS-DIO48 board into the Macintosh computer is very straightforward. There are no user configurable DIP-switch settings nor jumpers on the board which have to be set prior to installation.

The board should be installed in the computer in accordance with Apple Computer's recommendations concerning interface boards. The NBS-DIO48 board is designed to work in any of the available NuBus slots in the Macintosh II computer.

Following the installation of the board, the hardware verification program included with the board should be run in order to check correct operation. Operation of the hardware verification program is covered in the next section of the manual.

Section 3
Hardware Verification

Included on the disk which accompanies the card is an application (NBS-DIO48 CHECK) intended to be used to verify the correct operation of the NBS-DIO48 card hardware after installation. The program will check the contents of the PROM, and the I/O ports of the card.

The application requires a file named 'nbs-dio48 romimage' to be located in the folder where the 'NBS-DIO48 CHECK' program itself is located in order to function properly. This file contains an image of the driver code contained in the PROM located on the card. This image is used in order to verify the contents of the PROM. If upon launch, the application cannot locate the 'nbs-dio48 romimage' file, an alert message will be displayed informing the user of the problem. The application will quit after the user acknowledges the alert. It will be necessary to move the 'nbs-dio48 romimage' file into the folder where the NBS-DIO48 CHECK program is located and then restart the application in order to correct this problem.

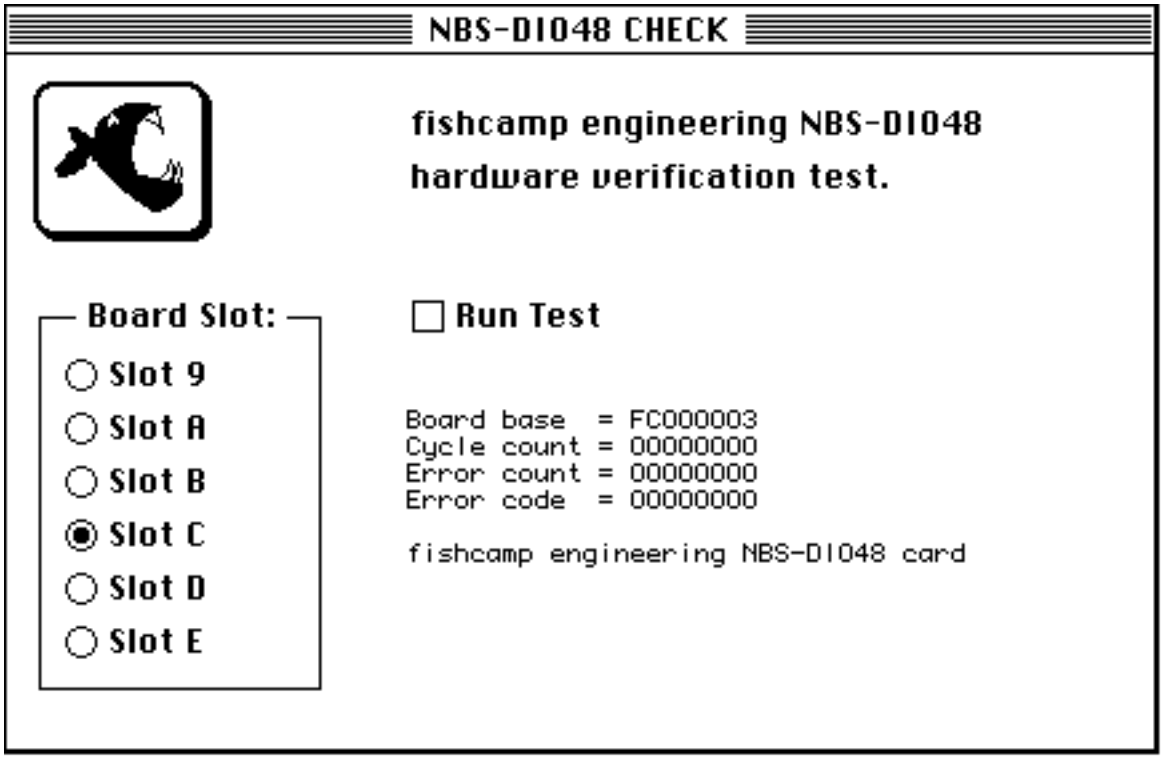


Figure 3.1 - NBS-DIO48 CHECK Window

Double-click on the NBS-DIO48 CHECK application icon to start the program. Figure 3.1 shows the window presented on the screen by the NBS-DIO48 CHECK program.

In order to run the test the user must first select the slot in which the NBS-DIO48 interface card is installed. The radio-button cluster labeled 'Board Slot:' should be

used to select the proper slot. After a slot number is chosen by the user the program will display, in a status line to the right of the radio-buttons, the official product name of the board installed in the slot. This name is the one which was registered by the card manufacturer with Apple Computer when the board was designed. All cards conforming to Apple Computer's design guidelines for interface cards will contain this name in their declaration ROM. If the system does not recognize that a card is installed in a particular slot, it will display a message to that effect in the status area of the window.

After the board slot has been chosen the test can then be started by checking the box marked 'Run Test' in the display. The program will then begin to run it's test routines. Each time the sequence of tests is run, the results of the test will be shown in the display window. If an error is detected then the 'Error code' line will provide information as to what portion of the test failed. Call fishcamp engineering if any error code other than the default `'00000000'` is displayed in the window. As long as the 'Run Test' check box is enabled, the application will continue to re-run the test. Any errors encountered will be accumulated in the 'Error count' field of the display. The 'Cycle count' line will display the total number of times the test was run.

The program will only allow the user to start the test if a slot has been selected which actually contains an NBS-DIO48 card. This implies that a certain amount of functionality be present in the card in order that the program can detect that the board is installed. If the card is completely non-functional the program will not even be able to detect the board's name and the card should be assumed to be faulty. Contact fishcamp engineering to arrange for repair.

After the verification program's tests have been run successfully, the NBS-DIO48 will be ready to use. Refer to the NBS-DIO48 Software Reference Manual for programming information regarding the use of the card.

This page intentionally left blank

Section 4
Theory of Operation

The NBS-DIO48 interface card is a single 4" X 7" printed circuit board with all of the required circuitry to interface correctly with the Macintosh II NuBus interface on the computer side, and a parallel digital device on the I/O side. Most of the circuitry on the board is used to handle the interface to the NuBus interface of the computer with only a small portion dedicated to handling the digital I/O port. All data transfers across the NuBus interface is made via 8-bit transfers over byte lane 3 of the NuBus. Only slave mode operation is supported over the NuBus with programmed I/O making all the data transfers.

NOTE

Figure 4.1 is a block diagram showing the key components of the NBS-DIO48 card. The schematic drawing for the card is reproduced in the appendices of this manual. In the following paragraphs, references to logic elements on the card are made. The reader should refer to the block diagram and the schematic for the card when reading the technical description.

The NuBus is a 32-bit interface with a multiplexed address/data bus. Along with the address/data bus lines are included several control signals which are used to time the transactions over the bus, facilitate de-multiplexing of the address and data lines, and provide address selection decoding . All data transfers are made by first de-multiplexing the bus into it's address and data components. Latches U7, U9, and U11 are used to store the de-multiplexed versions of the bus signals.

All timing for data transfers to or from the card over the NuBus is governed by the logic emulated in the two programmable logic (PAL) devices U8 and U10. These two devices form a state machine which demarcates the various states of a NuBus data transaction over the bus. All transactions take five NuBus clock cycles to complete. The state machine waits in state '0' until the address compare circuit, composed of U2 and U3 logic gates, detects that the upcoming data transfer is addressed to the board's own NuBus address. This triggers the state counter to start counting thru states '1', '2', '3', and '4' finally going into the resting state '0' again at the end of the transfer. Certain circuitry in the PALS decode the various states that the state machine traverses and generate timing signals and strobes used by other devices on the board. Refer to the timing diagrams in the appendices for a pictorial of the signals generated on the board.

Two of the signals generated by the PALS are the 'read' and 'write' strobes for the appropriate NuBus transfer. The PALS also take care of decoding the various NuBus addresses to generate the chip select signals for the I/O devices on the board. All devices on the card are memory mapped to distinct memory locations in the NuBus address space. The card maps the NuBus slot address space into four distinct sections:

- PROM
- Interrupt Mask Logic
- PPI controller registers
- Interrupt Logic

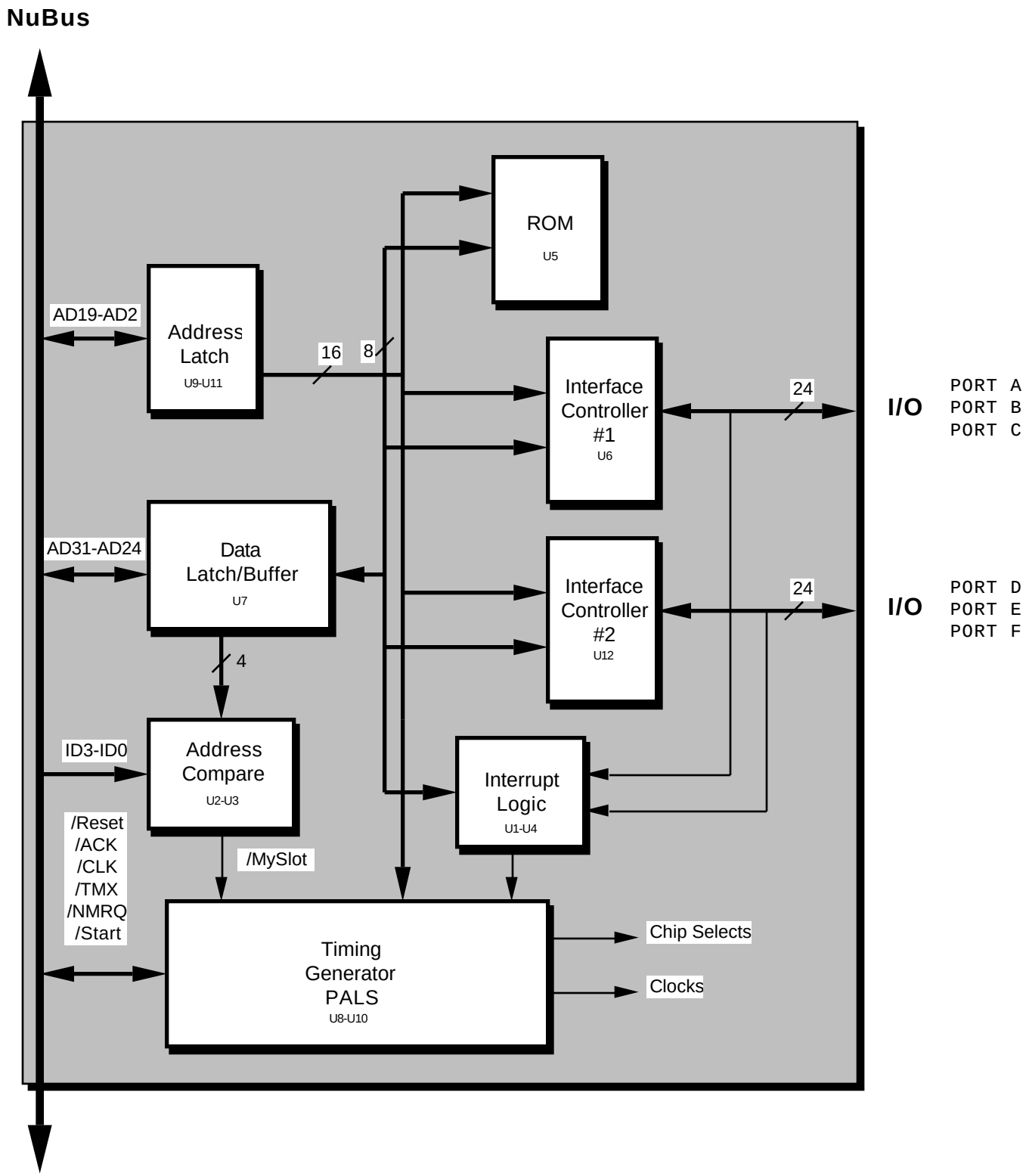


Figure 4.1 - NBS-DIO48 Block Diagram.

The first section occupies the upper portion of the address space allocated to the card in the NuBus slot address space and is used to address the contents of the PROM containing the system driver code for the card. This PROM has an 8K-byte total capacity. The Mac operating reads the driver code from this PROM into system memory at reset time and then executes the code out of system memory from then on. The PROM is usually never accessed after this.

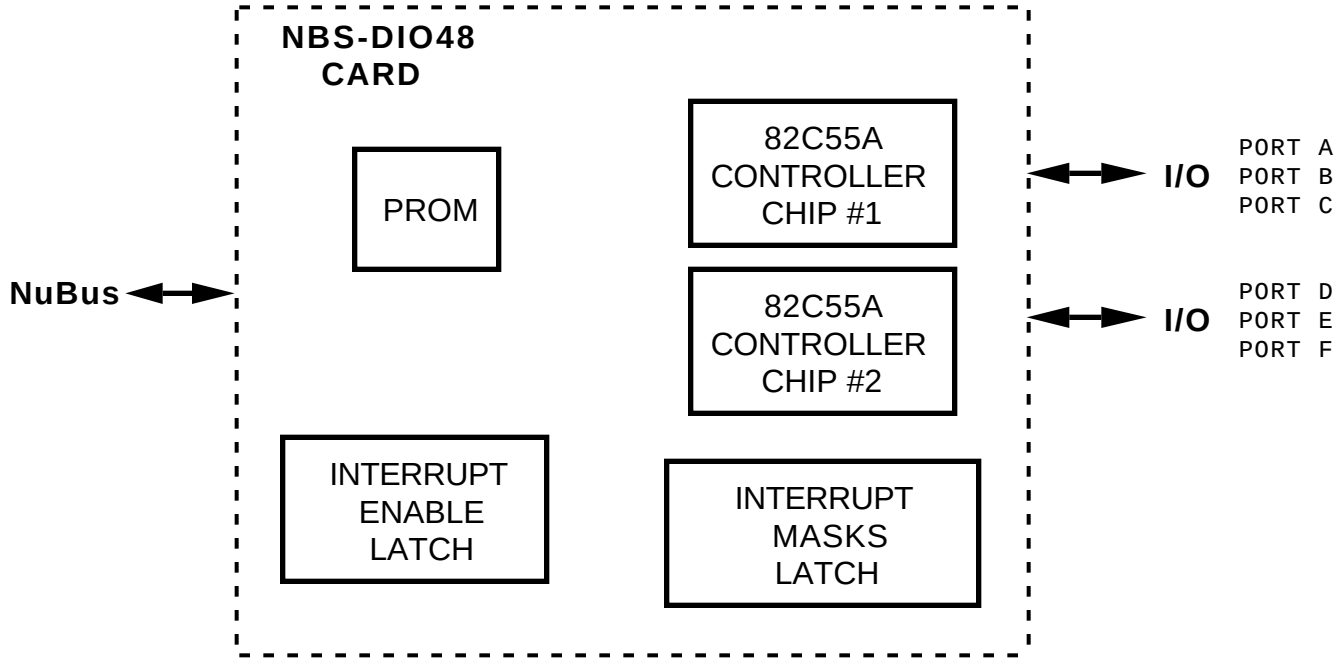


Figure 4.2 - NBS-DIO48 Logical Devices.

The second memory device on the card is an interrupt mask latch used to enable and disable any of the four possible interrupt sources on the NBS-DIO48 card. The latch occupies a single byte in the memory map and is a write-only hardware device. Only the four least significant bits of the latch are used on the card. A '1' written to any of these bits of the latch will enable the bit's respective interrupt source such that it will pass the interrupt on to the MAC's processor. A '0' will prevent the interrupt from interrupting the MAC. The interrupt sources are the 82C55A's PC0 and PC3 I/O lines. Refer to the Intel documentation on this device for information on how to use these interrupts. Figure 4.3 shows the mapping of the interrupt mask latch bits to the interrupt sources.

The third and most important block of memory addresses on the card map directly to the I/O registers of the 82C55A controller chips used on the board. There are two 82C55A chips on the NBS-DIO48 card. The chips data bus lines D7-D0 are mapped to the NuBus AD24-AD31 lines respectively. For definitions of the bits of the controller chip's registers consult the Intel documentation on the device.

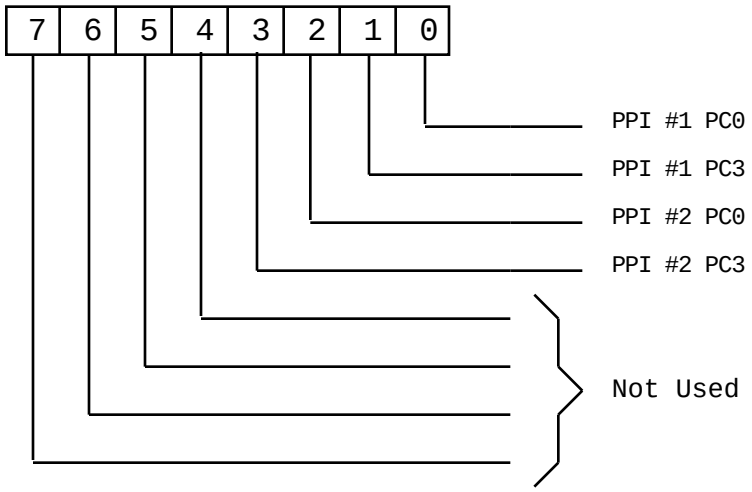


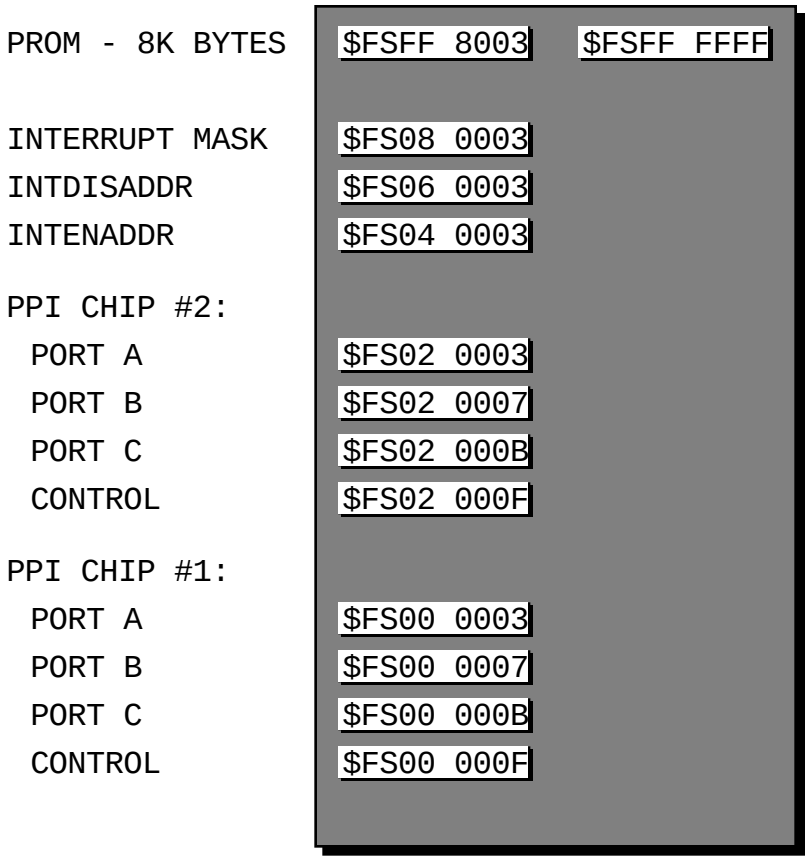
Figure 4.3 - Interrupt Mask Latch Bit Definition.

The last hardware device in the memory map is really two memory locations used in conjunction with each other to set the state of the interrupt enable latch on the card. The latch needs to be set if ANY interrupts from the NBS-DIO48 card are to be sent to the MAC's cpu. This latch is physically implemented internally to PAL U10. The hardware design of the card uses the state of the interrupt enable latch to qualify any interrupts from the 82C55A chips before passing them along to the NuBus 'NMRQ' interface line. Thus, to utilize interrupt operation on the NBS-DIO48 card, the application must first setup the mode properly for the 82C55A controller chip in order to enable the interrupt condition to be detected by the chip, and then secondly, set the interrupt mask bit for the particular interrupt desired as detailed in figure 4.3 above and, lastly, set the interrupt enable latch in order to pass the interrupt on to the MAC. Any access to 'intenaddr' will enable interrupts from the card. Similarly, any access to 'intdisaddr' will disable interrupts from the interface card. The interrupt enable latch is always reset (interrupts disabled) after a power-up or system reset of the MAC.

Because only byte lane three of the NuBus interface is used on the card, only every fourth memory location is valid in the NuBus address space. For instance, the 8K byte block of PROM is addressed starting at NuBus address $FSFF 8003. The next byte of PROM is located at address $FSFF 8007. And so on thru the remaining addresses. Application writers need to keep this in mind when writing the code for their program.

All I/O port lines from the two 82C55A chips used on the NBS-DIO48 card are brought out directly to the 'D' connector accessible from the back panel of the MAC when the card is installed in the computer. Each 82C55A chip provides 24 digital signal lines for use externally. The Intel documentation for the chip groups the I/O lines into three separate ports of 8 bits each. These ports are labeled 'Port A', 'Port B', and 'Port C'. On the NBS-DIO48 card, there are 6 ports labeled 'Port A', 'Port B', 'Port C', 'Port D', 'Port E', and 'Port F'. The 82C55A chip #1 (at base address $FS00 0003) maps its ports A thru C to the NBS-DIO48 card's ports A thru C respectively. The

82C55A chip #2 (at base address $FS02 0003) maps its ports A thru C to the NBS-DIO48 card's ports D thru F respectively. Refer to the schematic diagram in Appendix A.



NOTE:
Only byte lane-3 addresses used by card.

Figure 4.4 - NBS-DIO48 Memory Map Details

The card does not provide any signal conditioning above and beyond that of the 82C55A chips themselves. However, fused +5v power is provided on the I/O connector from the MAC's power supply for those users needing power for external signal conditioning circuitry. Users should limit the power draw from the +5v supply to be consistent with the power capacity of the NuBus interface specification. After taking into account the maximum power draw for the logic on the NBS-DIO48 card, calculations show that a maximum of 1.1A is available for external use. Power is accessible over two of the pins on the interface connector with each pin separately fused on the board for 1.0 Amp. The fuses are included for short circuit protection only.

CAUTION

Any application of the NBS-DIO48 card should not exceed the maximum voltage and current specifications of the 82C55A chip's interface lines. The user is urged to consult the Intel spec sheets for this chip. Under no circumstances should an external voltage be applied to any of the interface lines on the NBS-DIO48 I/O connector which is below -0.5V or above +5.5V as referenced from the GND signal on the connector.

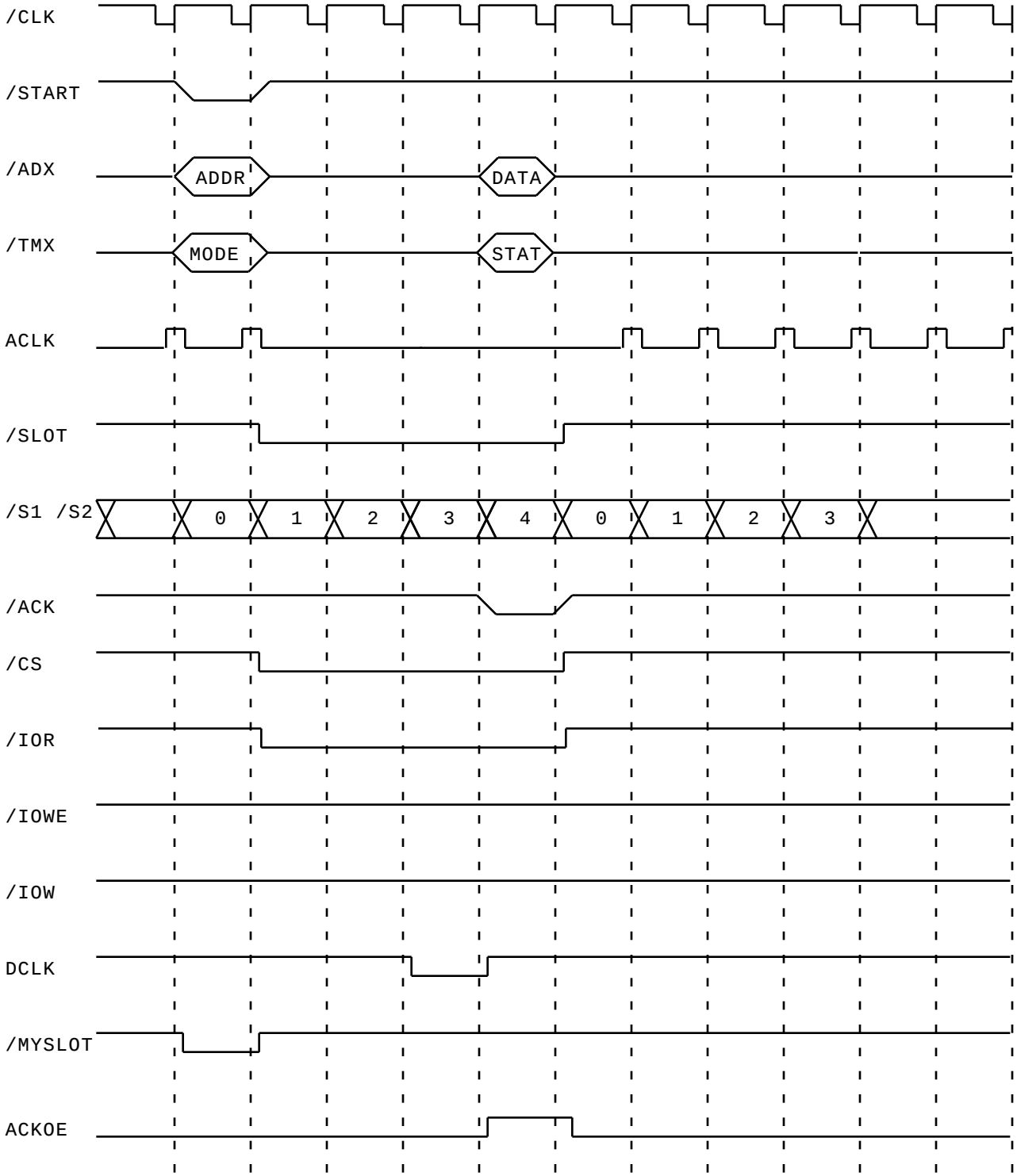
The appendices include copies of the schematic for the board as well as timing diagrams for important signals generated on the board. Also included are the source code listings for the two PAL devices discussed above. The reader should consult these documents for more detailed design information.

This page intentionally left blank

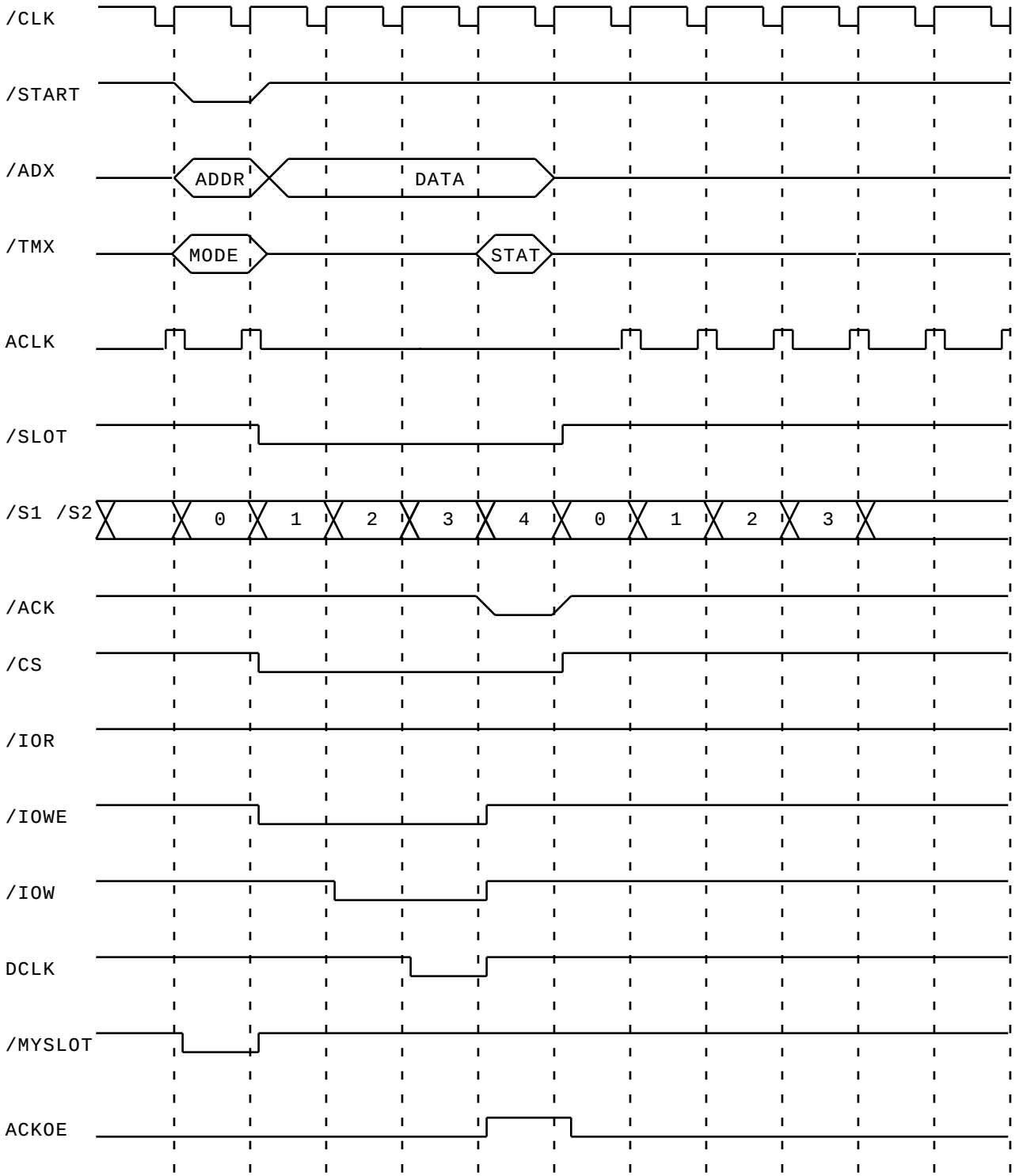
Appendix A
NBS-DIO48 Schematic

This page intentionally left blank

Appendix B
NBS-DIO48 Timing Diagrams



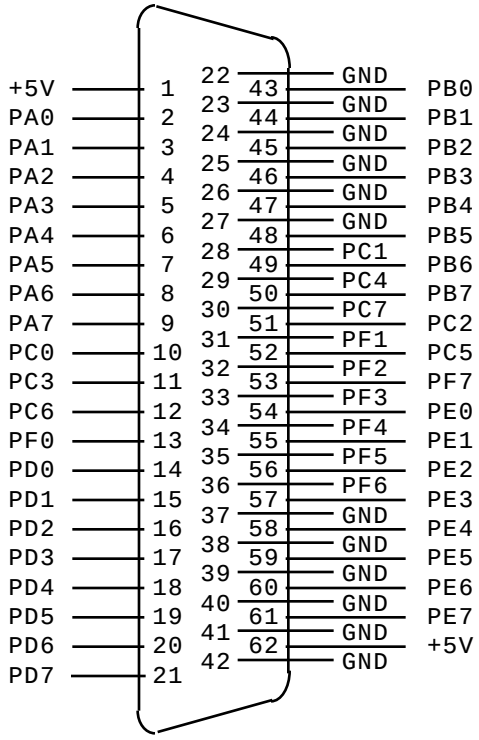
NBS-DIO48 READ Cycle Timing



NBS-DIO48 WRITE Cycle Timing

This page intentionally left blank

Appendix C
Connector Pinout



I/O Connector Pinout.

The connector used for I/O on the NBS-DIO48 card is a 62-pin high density 'D' type connector (AMP PN 748394-5). The following connector can be used to mate with this connector:

Connector housing - AMP PN 748367-1
Connector pins - AMP PN 748333-2

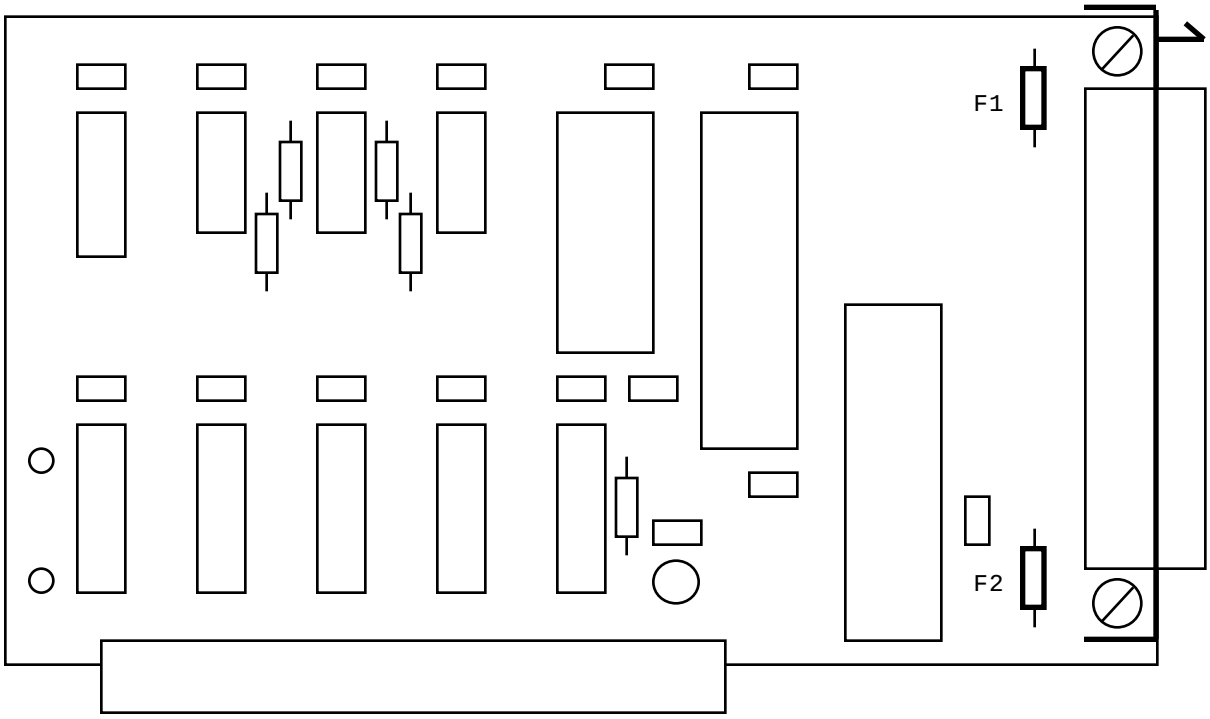
These parts can be ordered from:

AMP Incorporated
Harrisburg, PA 17105

Phone: (717) 564-0100
Fax: (717) 780-7112

Product Information Center (800) 522-6752

Appendix D
Fuse Type



Location of Fuses F1 and F2.

The above drawing shows the location of the two fuses which are in-line with the power pins on the customer I/O connector of the NBS-DIO48 card. For replacement purposes, the fuses used are the following type:

LITTLEFUZE- Picofuse Fast-Acting Type #265.001

These parts can be ordered from:

LITTLEFUZE
800 E. Northwest Highway
Des Plaines, IL 60016
(312) 824-1188